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SI-QSD EC chip

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Executive Summary

Purpose

The SI-QSDchip is a digital EC measurement system containing all necessary blocks for signal generation, AC current bias, voltage measurement, amplification, demodulation, filtering, digitalization, and communication.

The purpose of this document is to define the key specifications of each functional block. It supersedes the previous specification document (Rev. 0).

Document organization

The mainfunctions and target specifications are described for each functional block in the following chapters.

Table of Contents

1.

SI–QSD system overview

Typical use

The SI-QSD chip contains all the signal generation, signal acquisition and signal processing blocks needed to perform complex impedance measurements over a broad frequency range.

Active eddy current probe.

The high level of integration and miniaturisation of the SI-QSD chipmakes it the ideal component for an active eddy current probe combining both the measurement electronic and the sensor (coil) into a single probe body. This configuration targets high performance (improved immunity to interferences) or high level integration applications such as automated quality control, monitoring sensor or positioning sensors.

Electronic functional blocks

The SI-QSD is a complete digital single channel EC measurement system integrated onto a single CMOS chip. It contains all necessary functional blocks constituting an eddy current instrument. The block diagram of the SI-QSD chip is presented in a simplified schematic drawing, connected with a single coil.

Main functional blocks:

- Signal generation unit
- Dual-mode driver (current or voltage mode)
- HF preamplifier (input stage)
- Demodulators (I and Q downconversion mixers)
- Low-pass filter, balancing and gain block
- Analog-to-digital converters (ADCs)

Peripheral functional blocks:

- Digital communication (SPI)
- Voltage regulation (3.3 V) (not shown on the blok diagram)
- Temperature measurement (not shown on the block diagram)
- ESD protection

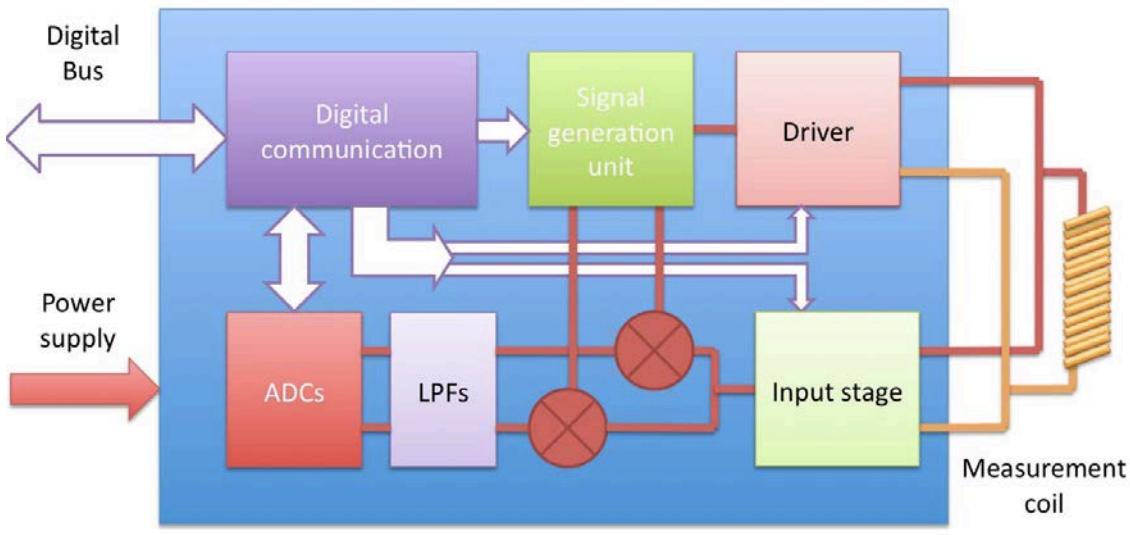

Figure 1.1: ***Block diagram of the SI-QSD chip with a single coil. The coil can be digitally reconfigured to act as absolute, driver or pick-up coil.***

In the following chapters, the main function and target specifications of each block are recapitulated.

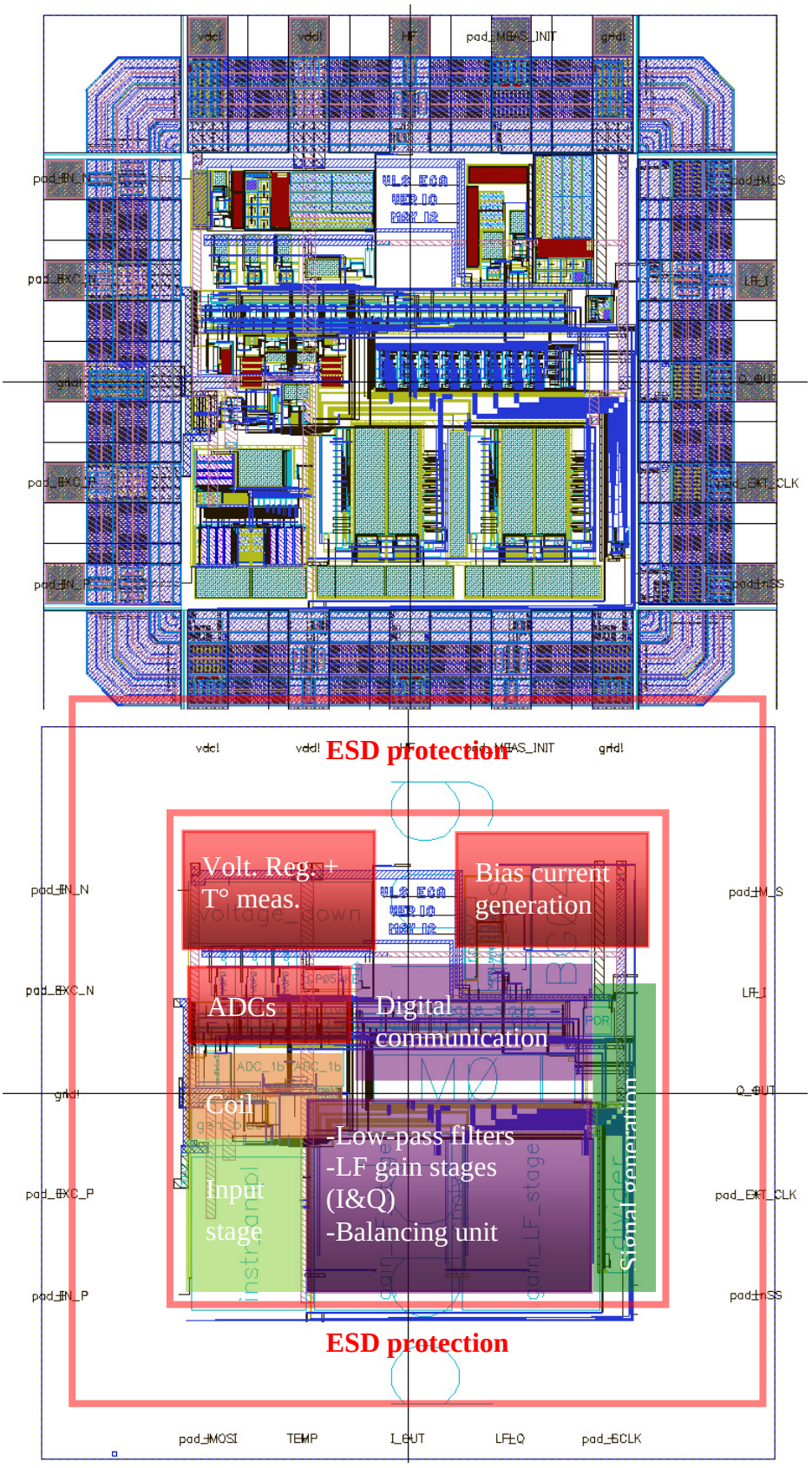

Figure 1.2: ***View of the final layout of the SI-QSD chip. The main functional blocks are highlighted.***

2.
Signal generation unit

Function

The function of this unit is to generate an excitation signal, as well as in-phase ant out-of-phase reference signals for demodulation. These can be used to generate an approximate sinein current-mode excitation or a square wave.

Specification

- 24 bits integer frequency division (formerly 16)
- Frequency range: 1 Hz to 6.5 MHz (formerly 380 Hz to 25 MHz)

3.
Dual-mode driver

Function

The function of this unit is to generate an excitation signal, as well as in-phase ant out-of-phase reference signals for demodulation. These can be used to generate an approximate sine in current-mode excitation or a square wave.

Specification

- 5V, 90mA excitation in voltage mode
- Adjustable sinusoidal current source
- High impedance mode: Impedance >> 100kOhms

4.
High frequency preamplifier

Function

The preamplifier provides an adjustable gain in front of the demodulators. It is a fully differential instrumentation designed to cope with high common-mode parasitic signals.

Specification

- High bandwidth: Up to 10 MHz at low gain
- Input swing: 1.0 - 4.5 V (worst case)
- Output swing: rail to rail (-0.1V)
- Low noise: 10 nV/sqrtHz at 100kHz, 25 nV/sqrtHz at 1kHz.
- Gain Steps: 2 to 20

5. Demodulators

Function

The function of the two demodulators is to perform the synchronous demodulation of the amplified input signal. Within this block, the amplified input signal is multiplied by an in-phase reference signal (I channel), and by a 90° out-of-phase reference (Q channel).

Specification

- Input bandwidth: DC - 10MHz
- Output bandwidth: DC - >10kHz

6.
Balancing, low-pass and LF amp

Function

The functions of balancing, low-pass filtering and final amplification are combined into a single block. The balancing allows an offset to be subtracted from the signal after demodulation. The resulting signal is amplified in the second gain stage, and simultaneously low-pass filtered to remove unwanted harmonics.

Specification

- Gain from 1 to 100 in 16 steps, 35.9% increase per step (formerly 1 to 20)
- 8-bit offset subtraction

7.

Analog-to-digital converters

Function

The function of this unit is to convert the voltage at the output of the LF amplifier into digital values. The tests of these units are the same as those used for the balancing, low-pass and amplification units, as no separate test point are available.

Specification

- 16-bit resolution
- No missing codes
- 500Hz – 3 kHz sampling rate

8. Additional modules

Temperature sensing and range

An analogue temperature sensor is integrated on-chip, with an output on the TEMP pad.

ESD protection

As can be seen on the layout of the SI-QSD chip, electrostatic discharge (ESD) protection is the largest block on the chip. It should ensure its long-term robustness in the field. It has been designed to comply with 0.35um HV ESD design rules, using tested cells provided by the foundry.